REMARKS

In the Outstanding Action, the Examiner rejected claims 1-15. Claims 1, 3, 7, and 9 have been amended. Claims 1-15 are now pending and submitted for consideration. Reconsideration of the application, as amended, is respectfully requested. The following remarks are submitted as a full and complete response to the Outstanding Action.

Section 102 Claim Rejections

The Examiner rejected Claims 1-15 under 35 U.S.C §102(a) as being anticipated by Tzeng et al., U.S. Patent No. 6,436,762 (Hereinafter Tzeng). This rejection is respectfully traversed.

Claim 1 recites a method for forming the bit-line contact of DRAM cell. Thed method comprises the following steps: providing a substrate comprising a plurality of control gates; forming a dielectric layer on said substrate; forming a patterned photoresist defining a first aperture on said dielectric layer; etching said dielectric layer by using said photoresist as a mask for exposing said substrate to form the bit-line contact window; filling said bit-line contact window with a conductive material to form the bit-line contact; planarizing the dielectric layer to expose the plurality of control gates; forming an isolation layer comprising a second aperture on said dielectric layer to exposure a portion of said bit-line contact; and forming a conductive layer on said isolation layer and filling up said second aperture.

In the prior art as shown in FIG. 1(e) of the present application, the isolation layer 109 with photoresist 104 defining a contact window pattern. The unprotected isolation layer 109 is etched away during the etching process (referring to page 1 of the specification). Because the control gates 102 are exposed to the isolation layer 109, the conduct material will touch the control gate when the conduct material is filled into the contact window 107. Thus, it possibly raises a short circuit issue. In the present invention, therefore, the bit-line contact window is formed by etching the dielectric layer. Then the dielectric layer is planarized to expose the plurality of control gates. An isolation layer comprising a second aperture is formed on the

dielectric layer to exposure a portion of the bit-line contact. In this way, the conductive layer filled into the second aperture will not touch the control gate since the isolation layer is not damaged during the etching process, thus the short circuit issue is prevented.

Tzeng deals with different problem comparing to the present invention. As we can see in FIG. 1-6 in Tzeng, the control gate is covered by conformal layer 22, 24, and then IPO layer 26. After forming the plug contacts 29, it is NOT planarized to expose the control gate and the second plug contact 29 is much higher than the control gate. Further, the ILD layer 40 is etched to forming the opening 3 to deal with the issue with capacitor top electrode 36 as shown in FIG. 6 in Tzeng. Referring to lines 52-56, col. 5 in Tzeng, it is recited that "the recessed openings 2' in the conformal conducting layer 36 and the bit-line contact openings 3". It is clearly Tzeng aligns ILD layer 40 to preventing short circuit between bit-line contact and the capacitor top electrode rather than the control gate.

Therefore, Tzeng at least fails to disclose planarizing the dielectric layer to expose the plurality of control gates. Also, Tzeng does not disclose and teach the issue between bit-line contact and the control gate. Accordingly, Applicant submits that the amended claim 1 satisfies the patentability requirement and is allowable.

Claims 2-15 respectively depend directly or indirectly on an allowable claim 1 and include further features. Therefore the above claims should be allowable over Tzeng. Withdrawal of the 35 U.S.C. § 102(a) rejection is therefore requested.

CONCLUSIONS

In light of the above amendments and remarks, Applicant respectfully submits that all pending claims 1-15 are in condition for allowance, and respectfully request the withdrawal of the rejections. Accordingly, a Notice of Allowance is respectfully requested.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone

number listed below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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